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10/534,430	07/18/2005	Anthony Spencer	0120-034	5040
42015	7590	01/07/2010	EXAMINER	
POTOMAC PATENT GROUP PLLC			CHOE, YONG J	
P. O. BOX 270			ART UNIT	PAPER NUMBER
FREDERICKSBURG, VA 22404			2185	
NOTIFICATION DATE		DELIVERY MODE		
01/07/2010		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tammy@ppglaw.com

<b>Office Action Summary</b>	<b>Application No.</b> 10/534,430	<b>Applicant(s)</b> SPENCER, ANTHONY
	<b>Examiner</b> YONG CHOE	<b>Art Unit</b> 2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 26 October 2009.
- 2a) This action is FINAL.      2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 19-46 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 19-46 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
- Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_
- 5) Notice of Informal Patent Application
- 6) Other: \_\_\_\_\_

**DETAILED ACTION**

1. The examiner acknowledges the applicant's submission of the amendment filed on 10/26/2009. At this point, claims 19, 32, 35, 36, 38 and 46 have been amended with claims 1-18 being canceled. Thus, claims 19-46 are pending in the instant application.
2. The objection to the claim 46 has been withdrawn as necessitated by amendment.
3. The rejection under the second paragraph of 35 U.S.C.112 to claim 46 has been withdrawn as necessitated by amendment.

***Response to Arguments***

4. Applicant's arguments with respect to claims 19-41 have been considered but are moot in view of the new ground(s) of rejection.
5. Applicant's arguments with respect to the rejection under the first paragraph of 35 U.S.C.112 to claims 39-41 have been fully considered and are persuasive. Thus, the rejection under the first paragraph of 35 U.S.C.112 to claims 39-41 has been withdrawn as necessitated by amendment.

***Continued Examination Under 37 CFR 1.114***

6. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the

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previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Applicant's submission filed on 10/26/2009 has been entered.

***Claim Rejections - 35 USC § 112***

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. **Claims 42-46** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The amended claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

**Regarding claims 42-45,** the limitation "wherein said state engine includes a plurality of state elements which comprise a plurality of local shared memories which provides a composite bandwidth that is a sum of all bandwidths associated with each one of said plurality of local shared memories" recited in 42-45 is not described in the applicants original disclosure.

**Regarding claim 46,** the limitation "a plurality of state engines, wherein one or more of said state engines are applied to a system bus and wherein said one or more of said state engines operate separately from each other" recited in 46 is not described in the applicants original disclosure.

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. **Claims 19-40** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Steely, Jr. et al. (US Patent No.: US 6088771)** in view of **Dieffenderfer et al. (US Patent No.: US 5822608)** and further in view of **Wang et al. (US Publication No.: US 2002/0062415)**.

**Regarding independent claims 19,32,35,37 and 38,** Steely discloses a state engine (Fig.2: switch 200) receiving multiple requests from a multiple processor system (Fig.2: multiple processor system) for a shared state (Fig.2: shared memory 150), the state engine (Fig.2: switch 200) comprising:

at least one state element (Fig.2: arbiter 240) means, said at least one state element (Fig.2: arbiter 240) means adapted to operate, atomically, on said shared state (Fig.2: shared memory 150) in response to a request made by said multiple processor system (Fig.2: multiple processor system) (Fig.2; and col.9, lines 26-51; and col.10, lines 24-54: The switch receives multiple requests from multiple processors for shared memory and arbiter operates the requests

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received from multiple processors) (Fig.2 and col.6, lines 1-17: the coherence controller 180 and IOP 130 control the arbiter to operate data selected by the arbiter on shared memory through Arb bus 170), wherein

said request includes at least a command directing said at least one state element means on how to perform an operation on said shared state (Fig.2; and col.9, lines 26-51; and col.10, lines 24-54: The switch receives multiple requests from multiple processors for shared memory and arbiter operates the requests received from multiple processors) (Fig.2 and col.6, lines 1-17: the coherence controller 180 and IOP 130 control the arbiter to operate data selected by the arbiter on shared memory through Arb bus 170); and

a memory (Fig.2: the queues 212-220) connected to said at least one state element means and configured to store said shared state (Fig.2: the queues 212-220 that are configured to store shared data is included in switch 200 which includes arbiter 240. Thus the queues connected to the arbiter 240 are included in the switch).

Steely further teaches means to supply data to update said shared state (Fig.1: data is transferred from processors to the shared memory. Thus, the data is supplied to update the shared memory).

However, Steely does not specifically teach the request is made by said parallel processor.

Dieffenderfer teaches teach the request is made by said parallel processor. (Fig.4 and col.12, lines 51-53: Fig.4 illustrates a basic picket configuration of a plurality of parallel processors and memories, picket units,

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arranged in a row on a single silicon chip as part of a parallel array which may be configured as a SIMD subsystem.).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the parallel processor as taught by Dieffenderfer into multiple processor system with shared memory of Steely because each processor may execute a separate program operating on a separate data set (col.1 line 65 – col.2, line 3). Therefore, it would have been obvious to combine the parallel processor as taught by Dieffenderfer with multiple processor system with shared memory of Steely to obtain the invention.

Steely and Dieffenderfer do not specifically teach said operation including reading, modifying, and writing back said shared state.

However, Wang teaches said operation including reading, modifying, and writing back said shared state ([0022]: the arbiter 108 issues grant responses (126) to the DMA devices 120 to take over the data bus 106 for a memory access cycle to perform read, write, and modify operations on the shared memory buffer 104).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbiter for a memory access cycle to perform read, write, and modify operations on shared memory buffer taught by Wang into multiple processor system with shared memory of Steely as modified by Dieffenderfer in order to coordinate the access to the data bus efficiently for all DMA devices. Therefore, it would have been obvious to combine the arbiter for a memory access cycle to perform read, write, and modify operations on shared

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memory buffer taught by Wang with multiple processor system with shared memory of Steely as modified by Dieffenderfer to obtain the invention.

**Regarding claim 20,** Steely teaches wherein the operation performed by said at least one state element means is a single read-modify-write operation (col.6, lines 29-33: Probes include Forwarded Read (Frd) commands, Forwarded Read Modify commands and invalidate commands. Forwarded-Read-Modify is analogous to the read-write-modify operation).

**Regarding claim 21,** Steely teaches wherein said shared state comprises a single item of state (Fig.2: single shared memory 150).

**Regarding claim 22,** Steely teaches wherein said shared state comprises multiple items of state (col.10, lines 31-32: there may be multiple banks of the shared memory).

**Regarding claim 23,** Steely teaches wherein said state comprises a single storage location or a data structure in storage (Fig.2 and col.5, line 54: A shared data structure 160 is provided).

**Regarding claim 24,** Steely teaches wherein the operation performed by said at least one state element means is carried out as a fixed or hardwired operation (Fig.2: arbiter is implemented in hardware. Thus the arbiter (i.e., state element means) is carried out as a hardwired operation unless a programmed operation is mentioned).

**Regarding claim 25**, Steely teaches supplying data to update said shared state (col.4, lines 22-34: arbiter select a request received from multiple processor and update the shared memory).

**Regarding claim 26**, Steely teaches sending a command and data to said shared state, whereby said operation is programmable (col.1, lines 11-24).

**Regarding claim 27**, Steely teaches a plurality of said state element means organized into state cell means, whereby operations performed on said shared state are pipelined (see Fig.2 and col.4, lines 22-34: i.e., atomic ordering process).

**Regarding claim 28**, Steely teaches a plurality of said state cell means, whereby to allow multiple requests to be handled concurrently (col.10, lines 31-33: there may be multiple banks of the shared memory and multiple request queues per processor).

**Regarding claim 29**, Steely teaches input and output interconnect means providing access to and from said state cell means, a bus interface for said input and output interconnect means, said bus interface interfacing with a system bus and a control unit of a processing element for controlling accesses to said shared state (col.6, lines 61-67 and col.7, lines 1-12: FIG. 2 is a schematic block diagram of the local switch 200 comprising a plurality of ports 202-210, each of which is coupled to a respective processor (P1-P4) 102-108 and IOP 130 via a full-duplex, bi-directional clock forwarded data link. Each port includes a first-in, first-out (FIFO) input and output queue set; that is, each port includes a respective input (request) queue 212-220 for receiving, e.g., a memory reference

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request issued by its processor, a respective output (probe) queue 222-230 for receiving, e.g., a memory reference probe issued by system control logic associated with the switch, and a respective output (fill) queue 262-270 for receiving, e.g., requested data provided by another processor of the system. An arbiter 240 arbitrates among the input queues to grant access to the Arb bus 170 where the requests are ordered into a memory reference request stream. In the illustrative embodiment, the arbiter selects the requests stored in the input queues for access to the bus in accordance with an arbitration policy, such as a conventional round-robin algorithm).

**Regarding claim 30,** Steely teaches wherein each said state element means comprises local memory, and each field of a data record is stored in a respective memory of a respective state element means (col.5, lines 54-67).

**Regarding claim 31,** Dieffenderfer teaches wherein each said state element means comprises a local memory for said shared state, an arithmetic unit adapted to perform the operation on said state in said local memory, and command and control logic to control said operation (col.18, lines 1-12).

**Regarding claim 33,** Dieffenderfer teaches wherein said parallel processor is an array processor (see Fig.4).

**Regarding claim 34,** Dieffenderfer teaches wherein said array processor is a SIMD processor (Fig.4 and col.12, lines 51-53: Fig.4 illustrates a basic picket configuration of a plurality of parallel processors and memories, picket units, arranged in a row on a single silicon chip as part of a parallel array which may be configured as a SIMD subsystem.).

**Regarding claim 37,** Dieffenderfer teaches teach a parallel processor implemented on a single silicon chip (Fig.4 and col.12, lines 51-53: Fig.4 illustrates a basic picket configuration of a plurality of parallel processors and memories, picket units, arranged in a row on a single silicon chip as part of a parallel array which may be configured as a SIMD subsystem.).

**Regarding claim 39,** Steely teaches wherein said operation results in a change of said shared state (see Fig.2; and col.4, lines 22-34; and col.6, lines 29-33).

**Regarding claim 40,** Steely teaches wherein said state engine is a programmable entity capable of executing shared memory instructions (col.1, lines 11-24).

11. **Claim 41** is rejected under 35 U.S.C. 103(a) as being unpatentable over Steely, Jr. et al. (US Patent No.: US 6088771) in view of Dieffenderfer et al. (US Patent No.: US 5822608) and further in view of Wang et al. (US Publication No.: US 2002/0062415) and Tetrick (US Publication No.: US 2001/0021967).

**Regarding claim 41,** Steely, Dieffenderfer and Wang do not specifically teach said memory is within said state element.

However, Tetrick teaches said memory (i.e., queue) is within said state element (i.e., arbiter). ([0018]: The arbiter includes a queue for normal priority

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requests for using the address and data lines 235 and a high priority queue for using the address and data lines 235).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the arbiter including a queue as taught by Tetrick into multiple processor system with shared memory of Steely as modified by Dieffenderfer and Wang so that a high priority queue requests can be accessed first. Therefore, it would have been obvious to combine the arbiter including a queue as taught by Tetrick with multiple processor system with shared memory of Steely as modified by Dieffenderfer and Wang to obtain the invention.

### ***Conclusion***

12. Any inquiry concerning this communication should be directed to **Yong Choe** at telephone number **571-270-1053** or email to **yong.choe@uspto.gov**. The examiner can normally be reached on M-F 9:30am to 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Sanjiv Shah** can be reached on **571-272-4098**. Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public

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PMR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-irect.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Yong Choe/  
Examiner, Art Unit 2185

/Tuan V. Thai/  
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